24/72 PLUSPAT - (C) QUESTEL-ORBIT
PN - EP0817095 A2 19980107 [EP-817095]
PN2 - EP0817095 A3 19980826 [EP-817095]
TI - (A2) **Extended** symmetrical multiprocessor **architecture**
OTI - (A2) **Architecture** à multiprocesseurs étendue et symétrique
- (A2) Erweiterte symmetrische Multiprozessorarchitektur
LA - ENGLISH (ENG)
PA - (A2) SUN MICROSYSTEMS INC (US)
PA2 - (A3) SUN MICROSYSTEMS INC (US)
IN - (A2) HAGERSTEN ERIK E (US); HILL MARK D (US); SINGHAL ASHOK (US)
AP - EP97304797 19970630 [1997EP-0304797]
PR - US67536196 19960702 [1996US-0675361]
- US67536296 19960702 [1996US-0675362]
- US67536396 19960702 [1996US-0675363]
IC - (A2) **G06F-013/40 G06F-015/16**
EC - G06F-015/173
DS - DE FR GB IT NL SE
DT - Basic
CT - Cited in the search report
- US4240143(A)(Cat. A);EP524684(A)(Cat. A)
STG - (A2) Pub. Of applic. Without search report
STG2- (A3) Publi. Of search report
AB - An **architecture** and memory mapping technique for an **extended** multiprocessor (XMP) computer system are provided to overcome physical/electrical limitations of single bus **architecture** while maximizing bus bandwidth utilization. The XMP computer system includes **multiple** SMP **nodes** each including an XMP interface and a repeater **structure** . The SMP **nodes** are connected to each other by unidirectional point-to-point links. The repeater **structure** in each SMP **node** includes an upper level bus coupled to one or more transaction repeaters. Each transaction repeater broadcasts transactions to bus devices attached to separate lower level buses. Transactions originating in a particular SMP **node** are stored in a queue, whereas transactions originating in other SMP **nodes** bypass the incoming queue to the bus device. **Multiple** transactions may be simultaneously broadcast across the point-to-point link connections between the SMP **nodes** in a defined, uniform order. Each of the n SMP **nodes** is assigned 1/n of the total address space. Cache coherency information is stored for the memory in each SMP **node** .
Memory regions may be assigned to operate in one of three modes: normal, migratory, or replicate. When operating in normal mode, transaction to an address space assigned to a particular **node** are tried only locally in that **node** first. In migratory mode transactions are always sent globally. And in replicate mode duplicate copies of the replicate memory region are assigned to each SMP **node** so that transactions are always tried locally first, and only sent globally if an improper cache coherency state is returned.